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Quasi-cyclic LDPC codes using overlapping matrices and their layered decoders

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ABSTRACT

Quasi-cyclic (QC) low-density parity-check (LDPC) codes have the parity-check matrices consisting of circulant matrices. Since QC LDPC codes whose parity-check matrices consist of only circulant permutation matrices are difficult to support layered decoding and, at the same time, have a good degree distribution with respect to error correcting performance, adopting multi-weight circulant matrices to parity-check matrices is useful but it has not been much researched. In this paper, we propose a new code structure for QC LDPC codes with multi-weight circulant matrices by introducing overlapping matrices. This structure enables a system to operate on dual mode in an efficient manner, that is, a standard QC LDPC code is used when the channel is relatively good and an enhanced QC LDPC code adopting an overlapping matrix is used otherwise. We also propose a new dual mode parallel decoder which supports the layered decoding both for the standard QC LDPC codes and the enhanced QC LDPC codes. Simulation results show that QC LDPC codes with the proposed structure have considerably improved error correcting performance and decoding throughput.

1. Introduction

After the big success of the turbo codes [1] in 1993, error correcting codes which have capacity-approaching performance and the corresponding low-complexity decoding algorithm have been much researched. As a result, low-density parity-check (LDPC) codes were rediscovered by MacKay and Neal [2]. It is known that LDPC codes show good performance for a sufficiently large code length even though their parity-check matrices are randomly constructed to have a few 1's and mostly 0's.

Although they have the capacity-approaching performance, randomly constructed LDPC codes are not well suited for efficient hardware implementation. Thus, quasi-cyclic (QC) LDPC codes were introduced in [3] as one of structured codes based on circulant permutation matrices. QC LDPC codes [4,5] are encoded with shift registers in linear time and they require a small amount of memories for parity-check matrix descriptions, compared with randomly constructed LDPC codes. Moreover, using the parallel structure of the QC LDPC code, their decoder can increase the throughput by the size of a circulant permutation matrix.

QC LDPC codes are desired to support both parallel decoding and layered decoding which enhance the throughput of the decoder like IEEE802.16e standards [6]. When the parity-check matrices of QC LDPC codes consist of only circulant permutation matrices, adopting the layered decoding puts a limitation on the construction of the parity-check matrices, especially in determining the maximum variable node degree ($d_v^{\max}$) of the LDPC codes. More specifically, for good error correcting performance, $d_v^{\max}$ is desired to be large enough according to [7] so that we need to increase the number of row blocks in the parity-check matrices, which causes the reduction of the size of each circulant permutation matrix. The reduced size of the circulant permutation matrices restricts the freedom of designing the parity-check matrix and decreases the efficiency of decoder obtained from the parallel decoding. However, if the parity-check matrices are designed with multi-weight circulant matrices, $d_v^{\max}$ can have a large value while supporting the efficient parallel decoding and the layered decoding.

In this paper, we propose a new code structure for QC LDPC codes with multi-weight circulant matrices by introducing the overlapping matrices. This structure enables a system to operate on dual mode in an efficient manner, that is, a standard QC LDPC code is used when the channel is relatively good and an enhanced QC LDPC code adopting an overlapping matrix is used otherwise. We also propose a new dual mode parallel decoder which supports the layered

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decoding both for the standard QC LDPC codes and the enhanced QC LDPC codes.

It is noted that the idea of overlapping matrices was originally proposed in our patent [8] and the initial version of the proposed dual mode parallel decoder was briefly shown in our previous work [9]. Actually, some layered decoders for QC LDPC codes with multi-weight circulants were proposed in [10–13] to avoid data update conflicts which occur in decoding. In [10], a layered decoder for DVB-S2 LDPC codes was proposed and it can be used to decode QC LDPC codes with only double-weight circulant matrices and circulant permutation matrices. The layered decoders in [11,12] are more efficient than the one in [10] but they are still used for only double-weight circulant matrices. In [13], the authors proposed a layered decoder which can be used for parity-check matrices with circulant matrices of weight larger than 2. However, all these layered decoder considered only simultaneous check node message updates while our proposed decoder deals with sequential check node message updates. Note that our proposed layered decoder can also support the decoding of QC LDPC codes with circulant matrices of weight larger than 2.

This paper is organized as follows: in Section 2, it is shown that multi-weight circulant matrices are adequate for parity-check matrices to adopt a desired degree distribution and support the layered decoding, and the overlapping matrices are introduced. In Section 3, we propose a new decoder structure for QC LDPC codes with overlapping matrices to resolve memory conflicts which cannot be avoided by the conventional decoders. The simulation results are shown in Section 4 and concluding remarks are given in Section 5.

2. QC LDPC codes with overlapping matrices

2.1. QC LDPC codes and layered decoding

A binary QC LDPC code can be defined by its $m \times n$ parity-check matrix H as

$$H = \begin{bmatrix} P_{0,0} & P_{0,1} & \cdots & P_{0,n_b-1} \\ P_{1,0} & P_{1,1} & \cdots & P_{1,n_b-1} \\ \vdots & \vdots & \ddots & \vdots \\ P_{m_b-1,0} & P_{m_b-1,1} & \cdots & P_{m_b-1,n_b-1} \end{bmatrix}$$

where $n = z \cdot n_b$, $m = z \cdot m_b$, and $P_{i,j}$ is a $z \times z$ binary circulant matrix or a $z \times z$ zero matrix. In the case that H consists of only circulant permutation matrices and zero matrices, the $m \times n$ parity-check matrix H can be obtained by expanding a *base matrix* H_b of size $m_b \times n_b$ as in [6]. Examples of the base matrix for the QC LDPC codes are shown in Figs. 1(a) and 2(a). The expansion process can be done by replacing each empty entry in H_b with a $z \times z$ zero matrix and each non-negative integer entry with a $z \times z$ circulant permutation matrix. The non-negative integers in H_b represent the cyclic shift values of circulant permutation matrices.

Notation 1 *(Base matrix).* A base matrix H_b can be expressed by listing all the non-empty blocks as follows:

H_b: {(row block index 1, column block index 1; shift value 1), (row block index 2, column block index 2; shift value 2) . . .}.

Example 1. The base matrix in Fig. 1(b) can be expressed as

H_b : {(0, 0; 50), (3, 0; 47), (4, 0; 15), (6, 1; 39),
(7, 1; 47), (10, 1; 74), (8, 2; 78), (9, 2; 43),
(11, 2; 22), (1, 3; 41), (2, 3; 43), (5, 3; 59),
(8, 4; 0), (9, 4; 79), (11, 4; 11), (0, 6; 39),
(10, 8; 24), (2, 9; 83), (1, 10; 84), (4, 11; 18)}.

There are various layered decoding algorithms to achieve high throughput decoder. In this paper, we will only consider the check node partitioning [14,15] which is one of the layered decoding algorithms. However, our proposed structure which will be illustrated soon can also be applied to other layered decoding algorithms. To support the check node partitioning, two or more groups of check nodes which do not share variable nodes are simultaneously processed in decoding. Fig. 1(a) shows that the variable nodes connected to the check nodes in the first row block form a disjoint set with the variable nodes connected to the check nodes in the third row block. In this case, all the check nodes in the first and the third row blocks can simultaneously update message vectors in the log-likelihood ratio (LLR) memories of the corresponding variable nodes without any conflicts. In the viewpoint of code construction, if the parity-check matrices consist of only circulant permutation matrices and zero matrices, $d_v^{\max}$ should be kept less than or equal to m_b/e for the layered decoding where e denotes the number of row blocks in each decoding layer. This restriction reduces the degree of freedom in determining the degree distribution and $d_v^{\max}$, which hinders finding good QC LDPC codes.

2.2. Overlapping matrices for the parity-check matrices with multi-weight circulant matrices

In this subsection, a new code structure for QC LDPC codes with parity-check matrices containing multi-weight circulant matrices will be proposed. In the parity-check matrices of QC LDPC codes, a column block containing multi-weight circulant matrices has more zero matrices than the one consisting of only circulant permutation matrices and zero matrices under the same column-weight. Thus, adopting multi-weight circulant matrices enables us to flexibly choose $d_v^{\max}$ of the QC LDPC codes and improve the throughput of the layered decoding.

Consider an $m \times n$ parity-check matrix consisting of $z \times z$ circulant matrices and zero matrices. Let $w_{\max}$ denote the largest

83					94	55					7	0											
			10		27					79			0	0									
			37						22					0	0								
25						65	61								0	0							
41										72							0	0					
			82						46			0						0	0				
	95							53											0	0			
	73				11					2										0	0		
		24		51			12														0	0	
		93		72							70											0	0
	7							65															0	0
		66		26			43					7												0

(a) The base matrix of a foundation matrix

50						39																	
			41								84												
			43							83													
47																							
15											18												
			59																				
	39																						
	47																						
		78		0																			
		43		79																			
	74								24														
		22		11																			

(b) The base matrix of an overlapping matrix

Fig. 1. The proposed code structure for a QC LDPC code with $R = 1/2$.

6	38	3	93				30			86			38		11		46	48	0				
62		19	84			78		15					45	23	32	30			0	0			
71		55			66	45	79		78					22	55	70				0	0		
	61			9	73		64		39	61	43						32	0			0	0	
				32	52	55		95	22		51	24		44								0	0
	63		88	20				6		56	16	71	53				26	48					0

(a) The base matrix of a foundation matrix.

							80			6			90		20								
38			66			47										94							
		31							41							27							
	94				92						92												
								70				37		4									
				12								10				82							

(b) The base matrix of an overlapping matrix.

Fig. 2. The proposed code structure for a QC LDPC code with $R = 3/4$.

weight of those circulant matrices. Then, the parity-check matrix can be decomposed into $w_{\max}$ $m \times n$ component matrices each of which consists of $z \times z$ circulant permutation matrices and $z \times z$ zero matrices such that the modulo-2 sum of the $w_{\max}$ $m \times n$ matrices is equal to the parity-check matrix. Note that this kind of representation is not unique. Let one of the component matrices, called the *foundation matrix*, have circulant permutation matrices as many as possible and the other $w_{\max} - 1$ component matrices are called *overlapping matrices*. Some examples of the base matrices of the foundation matrix and the overlapping matrix for QC LDPC codes are given in Figs. 1 and 2. Note that design criteria of good QC LDPC codes with multi-weight circulant matrices are not dealt with in this paper, which is another good research topic.

The proposed QC LDPC code structure, that is, dividing a parity-check matrix with multi-weight circulant matrices into a foundation matrix and overlapping matrices is adequate for dual-mode communication systems. Assume that a parity-check matrix with multi-weight circulant matrices is designed such that the foundation matrix is first constructed to have good error-correcting performance and then the overlapping matrices are constructed for the whole parity-check matrix to have good error-correcting performance. Then, the QC LDPC code whose parity-check matrix is the foundation matrix can be used on standard mode and the QC LDPC code whose parity-check matrix is the modulo-2 sum of the foundation matrix and the overlapping matrices can be used on enhanced mode in the wireless communication systems. We will call the former the *standard QC LDPC code* and the latter the *enhanced QC LDPC code* in the dual-mode communication systems.

3. New decoder structure for the proposed QC LDPC codes

3.1. Conventional parallel decoders

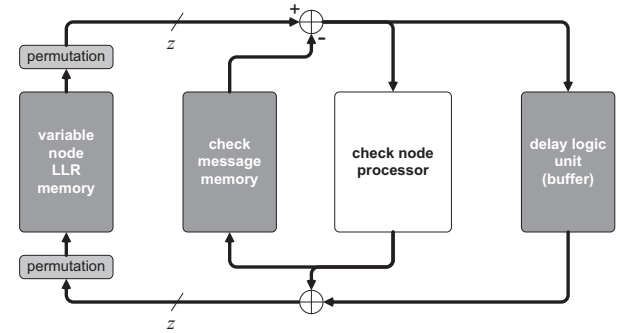
Conventional decoders supporting z-parallelism of QC LDPC codes whose parity-check matrices consist of only circulant permutation matrices and zero matrices in Fig. 3(a) operate on the base matrices of the codes, where z is the block size. They are composed of z copies of the constituent decoders having the identical structure and process the LLR message vectors of size z.

The operations in the conventional check node processing are given in Fig. 4(a). A check node is placed at the center and four neighbor variable nodes are connected to the check node. The left part of Fig. 4(a) shows the state of the LLR and the edge memories before check node operations. Note that the stored data in the LLR memories of the corresponding variable node blocks are not the individual message vectors but the sum-ups of all the message vectors from the neighboring check node blocks. The message vector from one of the neighboring variable node blocks can be calculated by subtracting message vector stored in the edge memory from the sum-up stored in the LLR memory of the corresponding variable node block. After the check node processing is performed with the message vectors from the neighboring variable node blocks, the resulting check node message vectors are stored in the edge memories. These message vectors are also added to the previous message vectors from the corresponding variable node blocks and updated on the LLR memories that belong to those variable node blocks. These operations are conducted over all the check nodes in a block by block manner.

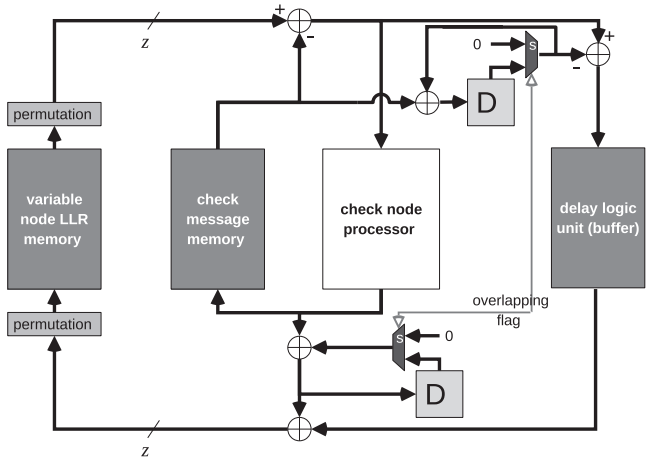
Example 2 *(Conventional check node processing).* To obtain the check node message vector 'A' for the top left variable node in Fig. 4(a), the check node operation is conducted on the message vectors 'f', 'g', and 'h' from all the other variable nodes. Each of these message vectors is obtained respectively by subtracting the outgoing message vectors 'b', 'c', and 'd' at the previous iteration from the sum-ups 'b + f', 'c + g', and 'd + h' stored in the LLR memories. Remaining check node message vectors 'B', 'C', and 'D' can also be obtained according to the same manner described above.

3.2. New parallel decoder structure

The above conventional decoder supporting z-parallelism of the QC LDPC codes can cause a problem for the QC LDPC codes with multi-weight circulant matrices adopting the proposed code structure when check node group updates along the multiple edges

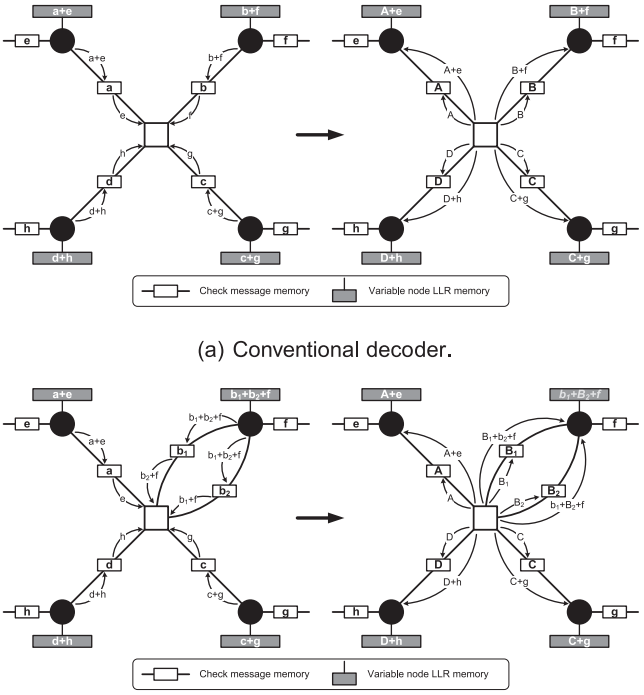


(a) The conventional decoder.



(b) The proposed decoder with sequential check node group update.

Fig. 3. Decoders supporting z-parallelism of QC LDPC codes.



(a) Conventional decoder.

(b) Memory conflict with overlapping matrix by sequential check node group update.

Fig. 4. Message update process.

introduced by overlapping matrices are sequentially conducted. In Fig. 4(b), there are multiple edges between the check node block and the top right variable node block. Each of the multiple edges has the message vector either 'b_1' or 'b_2' in the edge memory stored in the previous iteration, respectively. As the conventional decoder overwrites the lately updated message vector '$b_1 + B_2 + f$' on the LLR memory, previously updated message vector '$B_1 + b_2 + f$' is lost.

To solve the above memory conflict in the sequential check node group update process, a small number of additional memory spaces in the check node blocks are required for updating the LLR message vectors over the multiple edges. The LLR memory of the variable node block over the multiple edges should include all the changes in the updated message vectors to avoid memory conflicts. To do so, the check node processor requires temporary memories to keep the accumulation of the previously updated messages. The block diagram of the proposed decoder is given in Fig. 3(b). Note that just two memories "D" in Fig. 3(b) are required, no matter how many multiple edges are between each check node block and its neighboring variable node blocks. When the multiple edges are detected, that is, for an enhanced QC LDPC code, the overlapping flag is activated after the previous message vector is updated. And the proposed decoder acts as a conventional decoder for a standard QC LDPC code if the overlapping flag is inactive. For this reason, the proposed decoder not only supports dual mode, but also is compatible with the conventional QC LDPC codes whose parity-check matrices consist of only circulant permutation matrices and zero matrices.

4. Simulation results

4.1. Code performance

To show the performance improvement of the QC LDPC codes with the proposed code structure, three QC LDPC codes are compared. The half-rate QC LDPC code with $n = 2304$ in IEEE802.16e

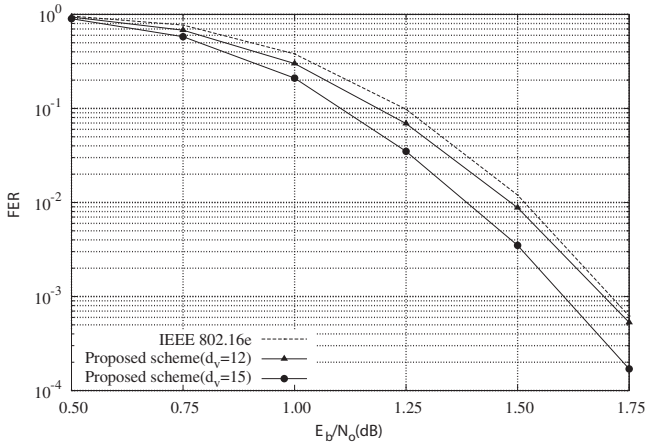


Fig. 5. Performance comparison of the QC LDPC codes with $n = 2304$ and $R = 1/2$.

standards [6] is used as the first QC LDPC code. The second and the third QC LDPC codes have the parity-check matrix of the half-rate QC LDPC code with $n = 2304$ as their foundation matrix in common. The second QC LDPC code has one overlapping matrix $H_b^{o_2}$ and the third QC LDPC code has two overlapping matrices $H_b^{o_{3,1}}$ and $H_b^{o_{3,2}}$ as below.

$$H_b^{o_2}: \{(1,7;13),(2,7;43),(5,7;95),(8,7;61),(9,7;79),(11,7;64),(0,9;25),(3,9;64),(4,9;82),(6,9;56),(7,9;91),(10,9;0),(1,11;49),(2,11;35),(5,11;16),(8,11;81),(9,11;2),(11,11;50)\}$$

$$H_b^{o_{3,1}}: \{(0,9;11),(1,11;25),(2,11;33),(3,9;45),(4,9;60),(5,11;81),(6,9;30),(7,9;61),(8,11;55),(9,11;78),(10,9;59),(11,11;34)\}$$

$$H_b^{o_{3,2}}: \{(2,11;61),(6,9;67),(7,9;3),(9,11;14),(10,9;94),(11,11;70)\}.$$

From the base matrices $H_b^{o_2}$, $H_b^{o_{3,1}}$, and $H_b^{o_{3,2}}$, we can see that the second QC LDPC code has $d_v^{\max} = 12$ and the third QC LDPC code has $d_v^{\max} = 15$.

As shown in Fig. 5, the bigger the maximum variable node degree is, the better the performance is. This result implies the natural fact that better performance can be achieved by increasing computational complexity, however, we want to point out that the overlapping matrices give rise to improvement of error correcting performance without change of the original code under the same foundation matrix and that this performance improvement can be obtained without throughput loss for the layered decoder.

4.2. Decoding throughput

Two QC LDPC codes with the proposed code structure designed to show improvement on the throughput of layered decoders are given in Figs. 1 and 2. The QC LDPC codes have the same degree distribution and number of edges with $R = 1/2$ and $R = 2/3$ QC LDPC codes in IEEE802.16e standards, respectively. The QC LDPC codes with $R = 1/2$ and $R = 2/3$ in IEEE802.16e standards have 2 row blocks in each decoding layer. On the other hand, four row blocks of the $R = 1/2$ codes in Fig. 1 and two row blocks of the $R = 3/4$ codes in Fig. 2 constructed by following the proposed code structure can be processed simultaneously in the layered decoder, respectively. More precisely, each of the (0, 2, 8, 10), (3, 5, 7, 9), and (1, 4, 6, 11) row blocks of the matrices in Fig. 1 can be processed

simultaneously and each of the (0, 4), (1, 3), and (2, 5) row blocks of the matrices in Fig. 2 can be also processed simultaneously in the layered decoder. As a result, the decoding throughputs are improved by 1.5 and 2 times compared to the $R = 1/2$ and $R = 3/4$ QC LDPC codes in IEEE802.16e standards, respectively. Note that the FER performance of the proposed codes is almost identical to that of the codes in the IEEE802.16e standards and all these performances are obtained by using the same number of edges as the IEEE802.16e standards.

5. Conclusions

In this paper, we propose a new code structure for QC LDPC codes with multi-weight circulant matrices by introducing the foundation matrix and the overlapping matrices. The proposed code structure enables a system to efficiently operate on dual mode by providing both the standard QC LDPC code and the enhanced QC LDPC code. Moreover, a new parallel decoder structure is proposed for the QC LDPC codes with the proposed code structure and it is fully compatible with the conventional QC LDPC codes. The QC LDPC codes with the proposed code structure achieve good error correcting performance by properly adjusting the degree distribution while supporting the layered decoding. The QC LDPC codes with the proposed code structure also improve the throughput of the layered decoding by placing more row blocks in each decoding layer.

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